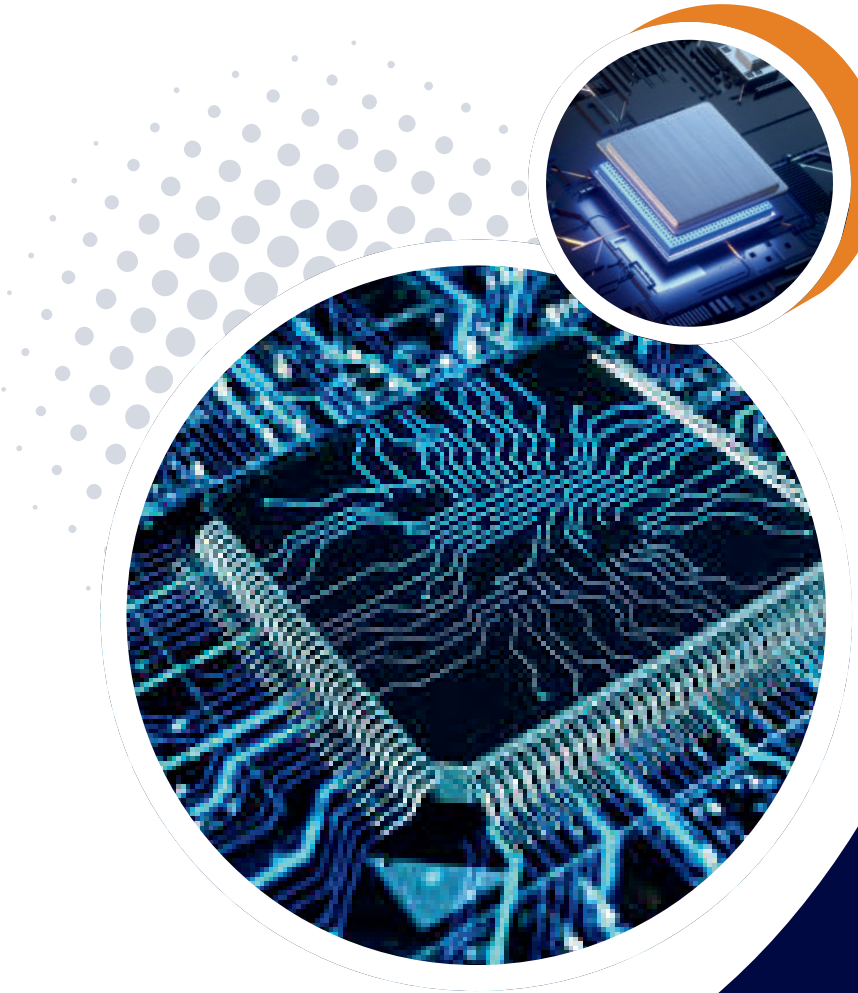
ChipXpert

THINK. DESIGN. OPTIMIZE

Advanced Design Verification

No Silicon Without Verification -
Become a Design Verification Engineer



www.chipxpert.in

About us

ChipXpert VLSI Training Institute is a premier institution dedicated to providing state-of-the-art training in Very-Large-Scale Integration (VLSI) design and semiconductor technology. With our commitment to bridging the gap between academic knowledge and industry requirements, we ensure aspiring engineers are fully prepared for successful careers in the fast-paced semiconductor and electronics industry. Our programs are designed by industry veterans, integrating theoretical foundations with practical expertise.

Eligibility Criteria

- B.Tech/B.E final-year students (ECE/EEE/Instrumentation).
- M.Tech/M.Sc 1st/2nd-year students (VLSI/Embeded).
- Graduates with completed B.Tech/M.Tech degrees.

Modes of Training Offered

- Classroom-Based Offline Training
- Interactive Online Training Sessions
- Industry-Focused Internship Program

Unique Features

- Guaranteed 100% Placement Assistance
- Impressive Hands-On 24/7 Labs & Projects
- Curriculum with Latest Industry Tools
- Corporate-Level Professional Training
- Flexible Training Modes with 24/7 eLearn Access
- Expert Trainers and Guest Sessions

Learning Outcome

- Understand the complete ASIC/SoC verification flow.
- Write effective SystemVerilog testbenches using OOP concepts.
- Implement Constrained Random Verification and Coverage-Driven Verification.
- Build reusable verification environments using UVM.
- Apply functional coverage and analyze results.
- Debug simulations using industry-standard tools.
- Use SVA for protocol and design checks.
- Gain real-time project experience to become job-ready.

Trainers Details

- 15+ years of industry experience in VLSI Design Verification, working with global semiconductor leaders like NVIDIA, Qualcomm, Intel, and AMD.
- Deep expertise in functional verification, including Testbench architecture, SystemVerilog, UVM, Constrained Random Verification, and Coverage-Driven Verification.
- Hands-on experience in verifying complex SoCs and IPs across multiple domains including processors, memory subsystems, and high-speed interfaces.
- Proficient in developing reusable UVM components such as drivers, monitors, agents, and scoreboards for scalable test environments.
- Strong background in functional and code coverage analysis, SystemVerilog Assertions (SVA), and debugging using waveform viewers like DVE and SimVision.
- Extensive tool knowledge in Synopsys VCS, Cadence Xcelium, and Mentor Questa, aligned with industry-standard verification flows.
- Training programs are designed to bridge the gap between academic learning and real-world industry demands, making learners job-ready for roles in design verification

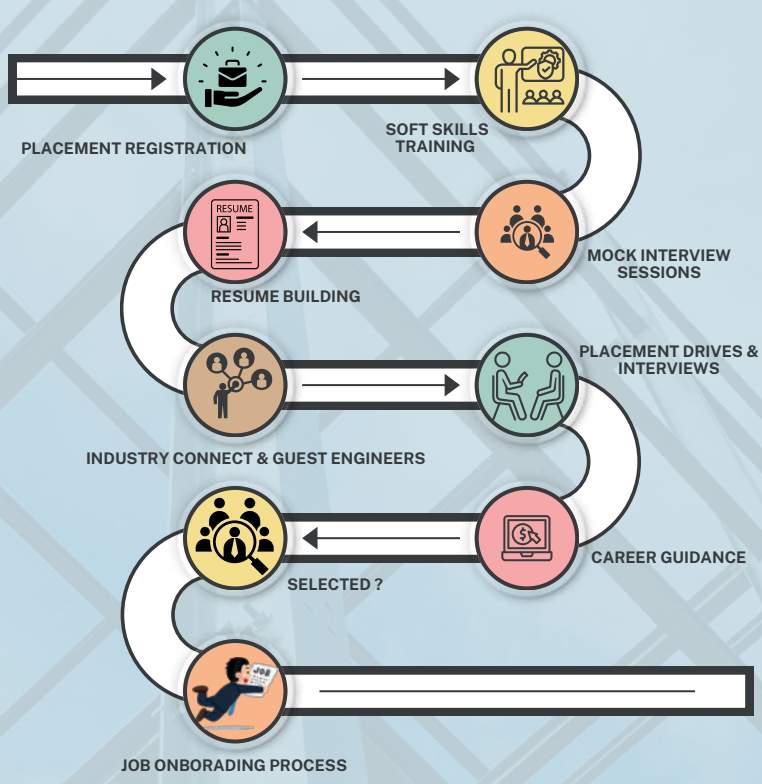
Physical Design Course Overview

ChipXpert proudly introduces its Advanced Design Verification Course, specially designed for students and professionals aspiring to build a rewarding career in the VLSI front-end verification domain. This course is curated by industry experts with over 15 years of experience at top semiconductor companies like NVIDIA, Qualcomm, Intel, and AMD. It offers comprehensive training on the complete ASIC/SoC verification flow, covering core topics such as SystemVerilog-based testbench development, Object-Oriented Programming (OOP), Constrained Random Verification, Functional Coverage, and the Universal Verification Methodology (UVM). Learners will also gain expertise in writing SystemVerilog Assertions (SVA), debugging with industry tools like Synopsys VCS, Cadence Xcelium, and Mentor Questa, and analyzing waveforms using tools like DVE and SimVision.

COURSE CURRICULUM

S.No	Module Name	Sub-Modules
1	Introduction to Electronics, MOSFET & CMOS Theory	- Introduction to Electronics and MOSFET Theory - Introduction to CMOS Process and Circuits
2	Digital Electronics	- Binary System and Boolean Algebra - Combinational Circuits - Sequential Circuits – Counters, State Machines, Shift Registers
3	Basics of UNIX/LINUX	- Introduction to Unix/Linux Commands - VI Editor Commands
4	Introduction to ASIC Design	- ASIC Design Flow Overview - Discussion of All Design Stages: Specification to GDSII
5	Introduction to Verilog	- Verilog Basics and Syntax - Gate-Level Modeling - Dataflow Modeling - Behavioral Modeling - Tasks and Functions
6	Introduction to DFT (Design for Testability)	- DFT Basics - Fault Modeling and Simulation - SCAN Design Concepts - Introduction to BIST
7	TCL Programming	- TCL Syntax and Variables - Control Structures and Loops - File I/O Operations - Procedures and Functions - TCL in EDA Tools - Best Practices
8	Synthesis	- Synthesis Flow: Inputs and Outputs - Constraint Development - Optimization Techniques (Unify, Preserve, Flatten) - Wireload Models (PLE, Physical, Spatial)
9	Static Timing Analysis (STA)	- Key Parameters: Transition/Slew, Capacitance, Power Analysis - Timing Models: NLDM, CCS, ECSM, LVF - Timing Checks: Setup, Hold, Recovery, Removal, Pulse Width, Clock Gating
10	SystemVerilog – Core Concepts	- Data Types, Operators, Arrays, Structures, Unions, Enumerations - Procedural Blocks (Initial, Always) - Classes, Inheritance, Polymorphism, Constructors
11	SystemVerilog – Advanced Verification	- Interfaces & Modports (Interface, Clocking Blocks, Modports) - Randomization (Constraints, In-line & Distribution) - Functional Coverage (Covergroups, Cross Coverage, Sampling) - Assertions (Immediate, Concurrent, Sequences)
12	UVM – Fundamentals	- Why UVM? - UVM Library Components - Simulation Phases - Factory and Configuration - Testbench Components: Agent, Driver, Sequencer, Monitor, Scoreboard - Sequences and Sequence Items
13	UVM – Advanced Concepts	- TLM 1.0 and 2.0 Basics - Ports, Exports, FIFOs - UVM Macros - Reports and Filtering - Callbacks - Factory Override - Virtual Sequences - UVM_REG: Register Models, Mirror/Update
14	Testbench Debugging & Tools	- Using Simulators (VCS, Questa, etc.) - Waveform Debugging - Breakpoints and Watch Windows
15	Coverage Planning & Final Project	- Coverage Plan Creation - Analysis and Closure - (AXI, UART, etc.) - Review and Debug Practices

Placement Process



MOCK INTERVIEWS WITH INDUSTRY EXPERTS

REAL-TME INDUSTRIAL PROJECT

COURSE COMPLETION CERTIFICATE

100+ Hiring Companies

Actel, Advanced Linear Devices, Inc., Agilent Technologies, AKM, Allegro, ALi, Altera, AMD, Analog Devices, Atmel, austriamicrosystems, Broadcom, Cirrus Logic, Conexant, Cypress, Exar, Fairchild Semiconductor, Halo Electronics, Inc., Holtek, hynix, intel, intersil, Hitachi, IDT, Infineon, International Rectifier, ISSI, KEC, level one, Lansdale Semiconductor Inc., Littelfuse, Linear Technology, MXIC, Marvell, maxim integrated, Micrel, Microlinear, Micron, Microchip, Micronas, Microsemi, molex, Motorola, National Semiconductor, NXP, OmniVision, Omron, ON Semiconductor, PLX, Pericom, Phoenix Contact, PMC, Qualcomm Incorporated

> CONTACT US

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